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Research Article

Fabrication of Lateral Polysilicon Gap of Less than 50 nm Using Conventional Lithography

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We report a thermal oxidation process for the fabrication of nanogaps of less than 50 nm in dimension. Nanogaps of this dimension are necessary to eliminate contributions from double-layer capacitance in the dielectric detection of protein or nucleic acid. The method combines conventional photolithography and pattern-size reduction techniques. The gaps are fabricated on polysilicon-coated silicon substrate with gold electrodes. The dimensions of the structure are determined by scanning electron microscopy (SEM). An electrical characterization of the structures by dielectric analyzer (DA) shows an improved conductivity as well as enhanced permittivity and capacity with the reduction of gap size, suggesting its potential applications in the detection of biomolecule with very low level of power supply. Two chrome Masks are used to complete the work: the first Mask is for the nanogap pattern and the second one is for the electrodes. An improved resolution of pattern size is obtained by controlling the oxidation time. The method expected to enable fabrication of nanogaps with a wide ranging designs and dimensions on different substrates. It is a simple and cost-effective method and does not require complicated nanolithography process for fabricating desired nanogaps in a reproducible fashion.

1. Introduction

The present invention relates to a process of forming an electrode with a desired nanogap. The development of a cost-effective, easily performable, and high-throughput technique for the fabrication of such structures is of great interests both for the possibility of increasing the device-packing density and the reduction of power consumption [1]. Such structures have potential applications in the next generation nanoelectronic devices, such as single electron transistors [1], metal/insulator tunnel transistors [2], nanowire transistors [3], nanotube- or nanoparticle-based devices [4, 5]. Chemical and biological nanosensors, biochips, and nanobioelectronics are other applications, which are progressing rapidly [4, 6–9]. The coupling of biomolecules with nanomaterials (nanoparticles, nanotubes, etc.) and nanostructures (e.g., nanoelectrodes, nanotransistors, nanogaps, nanopores, and nanochannels) of comparable dimensions might allow the creation of hybrid systems with unique functions and applications [4, 7, 10–16]. Such functional hybrid systems, originated from the "marriage" of biomolecules and nanoscaled transducers, provide powerful tools, not only for manipulation and detection, but also for the fundamental research of single biological molecule (DNA, immunoglobulins, proteins, and living cells).

The realization of different nanometer-sized structures has been demonstrated by advanced high-resolution nanolithography techniques, such as electron- or ion-beam lithography, focused ion-beam milling, scanning tunneling or atomic force microscopy, nanoimprint lithography, and different top-down fabrication techniques [17]. Although these techniques provide high resolution in generating different nanostructures, most of them are time-consuming, low-throughput, complicated, and expensive. If conventional photolithography could be applied to form nanometer-sized structures including line and space patterns, it would be highly advantageous. Therefore, recently, some non-conventional techniques in combination with conventional photolithography have been proposed for the preparation of nanoelectrodes, nanogaps, and other nanoscaled devices.

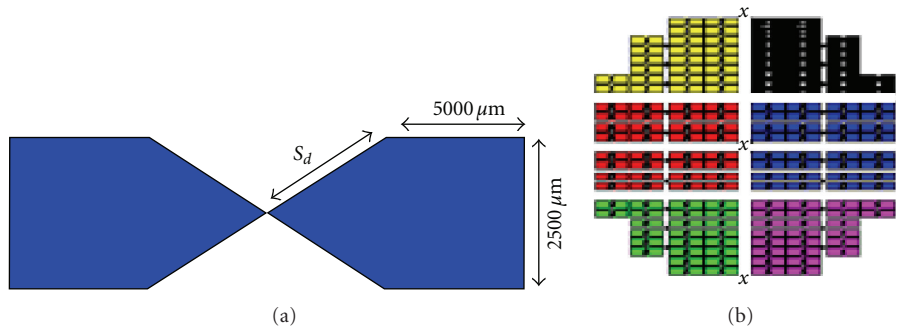

Figure 1: Schematic presentation of the first Mask with dimension specification (a) and the actual Mask on chrome glass (b).

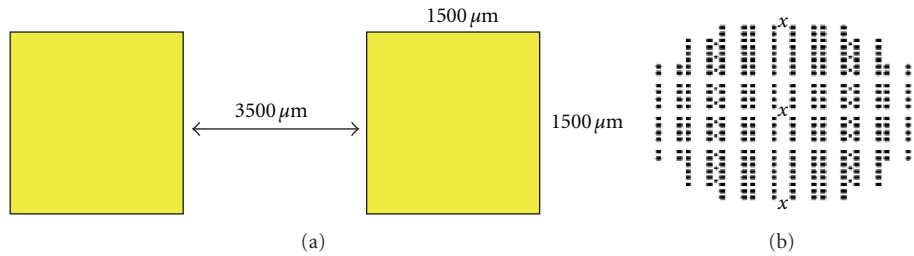

Figure 2: Design specification for Mask 2 (a) and the actual Mask on chrome glass (b).

These techniques include, for instance, a photoresist thermal reflow and shrinking [18] or photoresist ashing technique [19], a shadow evaporation process [20], a controlled size reduction using the oxidation of Si [21–23] or laser-assisted electrochemical etching [24], chemical-mechanical polishing [25], the decrease of separation between metallic electrodes by means of an electrodeposition from an electrolyte solution [26], methods that utilize a sidewall structure [27], a self-aligned plasma etching of a silicon dioxide layer and silicon substrate [28], or a lateral, partial anodic oxidation of the side edge of a photolithographically structured metallic film (e.g., Ti) [29], and techniques that use a silicon-on-insulator structure [30].

An alternative solution for the fabrication of self-aligned nanostructures by means of conventional photolithography combined with pattern-size reduction techniques has recently been proposed [31, 32]. The method of the thermal oxidation is displayed by patterning nanostructures with different sizes and layouts on a polysilicon-coated silicon material. The current report demonstrated the preparation of polysilicon nanogaps of less than 50 nm on a Si_3N_4–SiO_2–Si substrate. Less than 50 nm gap is expected to eliminate contributions from double-layer capacitance in the dielectric identification of protein, nucleic acid, or small molecule [33]. A number of methods for fabricating nanogaps have already been established. But our goal is to develop a cost-effective and easily performable fabrication technique that can be applied in batch production. We have proved the suitability of our method in such application by fabricating a gap size of 42 ± 5 nm on silicon substrate in a reproducible manner. Preliminary DA characterization data suggests that such structure can be used in biomolecule sensing with very low level of current supply.

2. Materials and Methods

2.1. Mask Design. A 100 mm p-type silicon wafer is used as a substrate to fabricate the nanogap structure. We design two masks: one for the polysilicon nanogap and the other for the gold electrode by AutoCAD software. The masks are printed onto a chrome glass surface and purchased from a commercial company (Photonic Pte. Limited, Singapore). We apply dry etching (reactive ion etching (RIE)) to fabricate the gap and wet etching (buffer oxide etching (BOE)) to pattern the electrode structures. The anisotropy of RIE is modeled, and the etching profiles are simulated [34].

Figure 1(a) shows the first Mask for nanogap generation with a length of 5000 μm and a width of 2500 μm. The chrome Mask with actual arrangement of device design is shown in Figure 1(b). It consists of 160 dies with 6 different layouts. The angle length of the end electrode is of 1/6th scale starting from 100 μm to 1100 μm with an increment of 100 μm for each unit of S_d length. This is simply for checking the best angle for the best nanogap formation after the etching process. The symbol S_d refers to the dimension of the side angle of the proposed nanogap. The sharpness of the nanogap proportionates to the dimension of S_d.

Figure 2(a) is a schematic device design of Mask 2 with 1500 μm of length and 1500 μm of width. The distance between the two rectangles is 3500 μm. The actual Mask is shown on the chrome glass Figure 2(b).

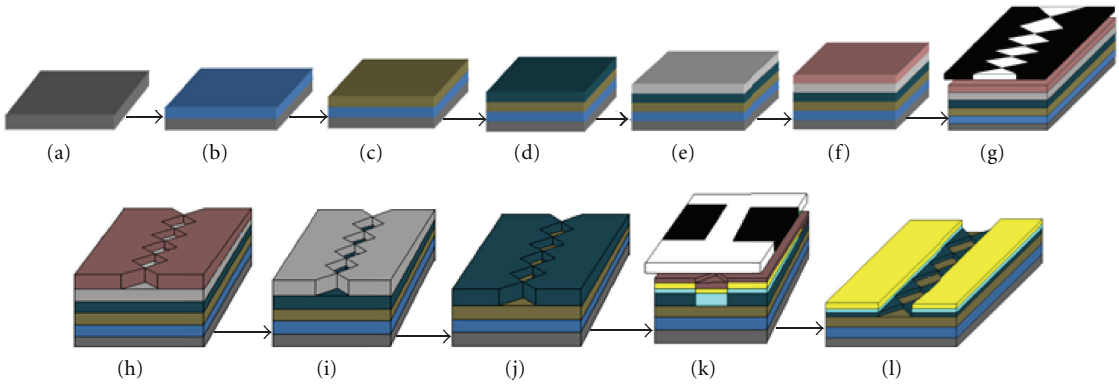

FIGURE 3: The process flow for the fabrication of polysilicon nanogap structure. (a) Silicon wafer starting material; (b) deposit of 50 nm SiO_2 layer; (c) deposit of 150 nm Si_3N_4 layer; (d) deposit of 2000 nm polysilicon layer; (e) deposit of 135 nm Al layer; (f) photoresist coating; (g) Mask 1 exposure; (h) the resist development; (i) wet etching for Al layer; (j) dry etching of polysilicon layer; (k) exposure of Mask 2 after depositing Ti/Au layer; (l) final device after wet etching for the Ti/Au electrode.

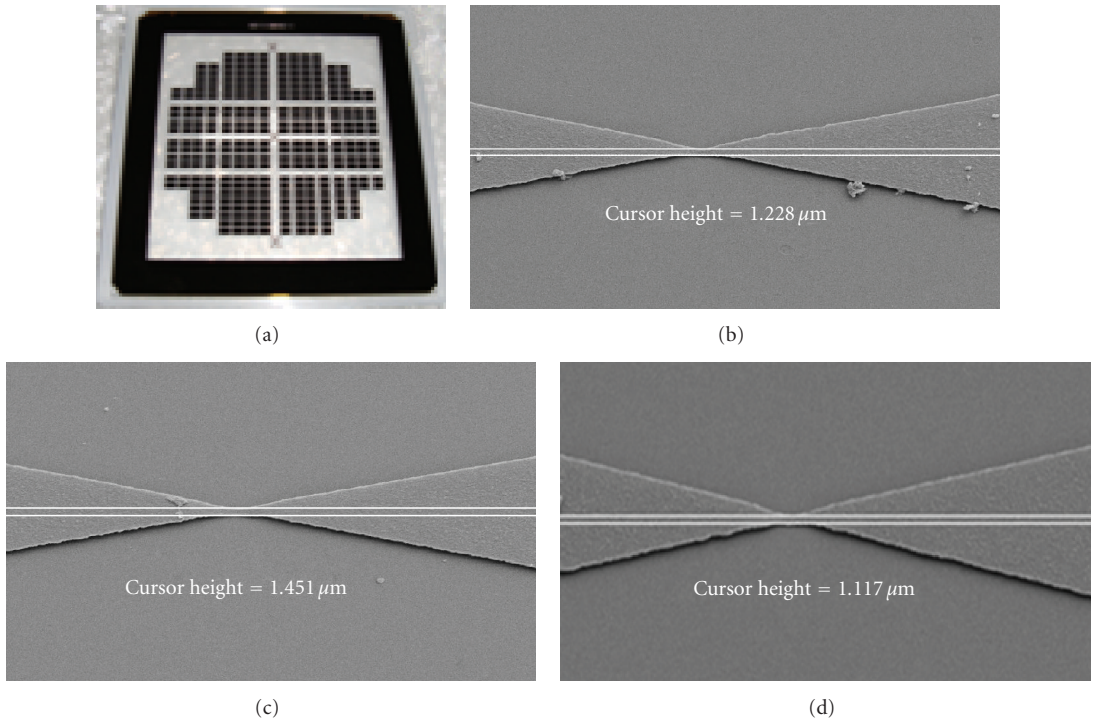

FIGURE 4: Photo Mask used in exposure process (a) SEM images of fabricated polysilicon pattern (b) before (c) after thermal oxidation treatment and (d) at the end of BOE.

2.2. Fabrication of Nanogap Structure. Figure 3 schematically shows the process flow for the fabrication of gold electrode with desired polysilicon nanogap on silicon substrate. The fabrication is started with the cleaning of the silicon wafer (a), followed by deposition of a 50 nm SiO_2 (b), and 150 nm Si_3N_4 (c), layers by plasma-enhanced chemical vapor deposition (PECVD) equipment. In the next step, a 2000 nm polysilicon layer (d) is deposited by low-power chemical vapor deposition (LPCVD) equipment. After that, a layer of 135 nm aluminum substrate (e) is placed as a hard Mask by physical vapor deposition (PVD) instrument to avoid damage to the polysilicon layer during the etching (RIE) process. The next is the photolithography process. A layer of positive photoresist of 1200 nm thickness (f) is applied on the aluminum substrate, and then exposed to ultraviolet light through Mask 1 (g). Following the development process (h), only the unexposed resist would remain. The wet-etching process of the aluminum layer (i), is performed before removing the resist. Subsequently, the dry-etching process (j), for the polysilicon layer is done to fabricate the nanogap by reduction of gap size. A layer of 150 nm gold substrate is deposited (k), over a 60 nm Ti layer. In the following step, the resist-coating process is applied before exposing Mask 2 and developing the resist, (k). Finally, the wet-etching process of

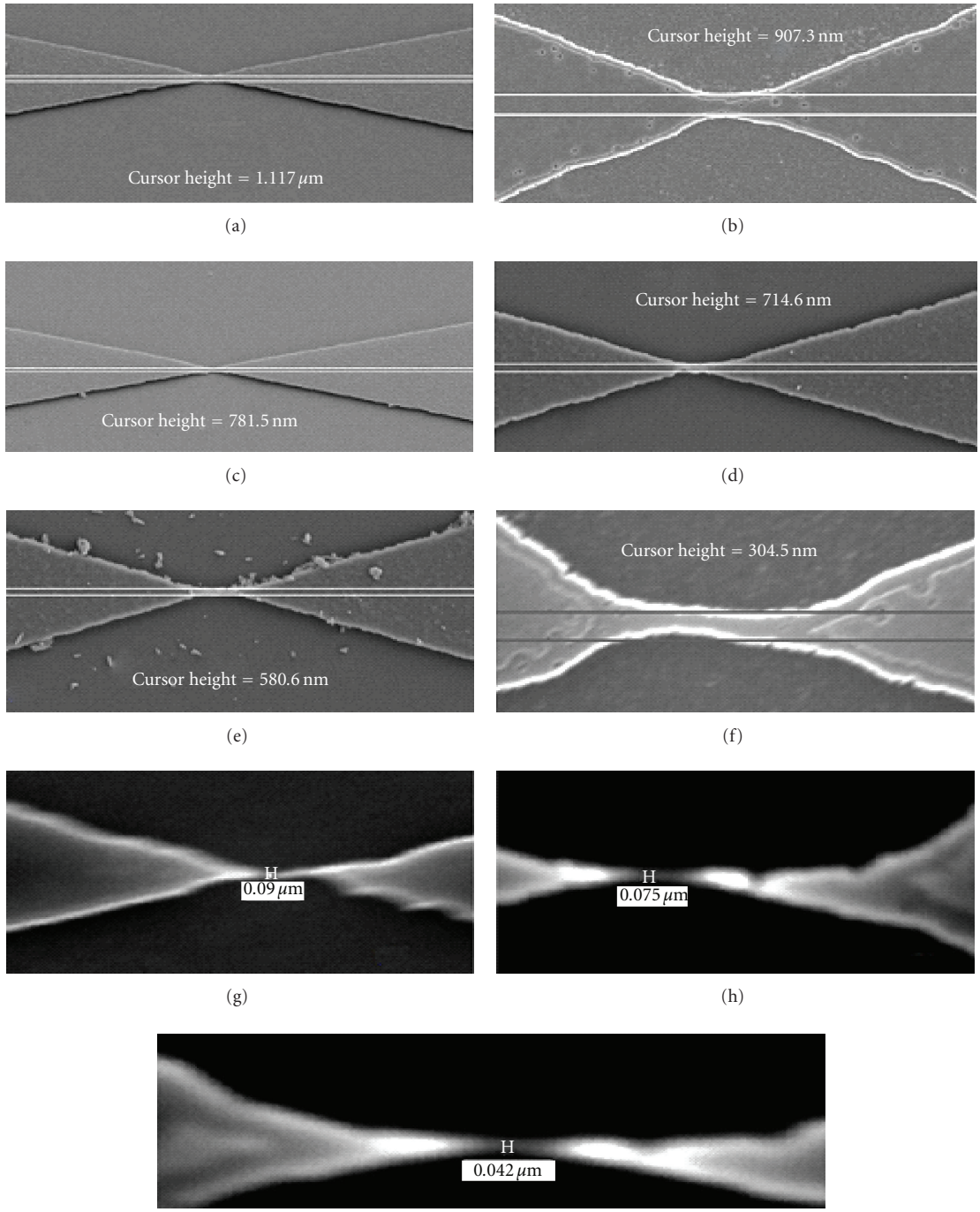

Figure 5: The SEM images of the nanopap structure after etching with BOE solution at the end of each thermal oxidation. Shown are the polysilicon layer at the end of the first to seventh cycles with 15 min of oxidation, from (a) to (g); 7th cycle with 10 min (h), and 5 min (i), of thermal oxidation.

the Ti/Au substrate is performed to obtain the gold electrode with the polysilicon nanogap (l).

Before fabricating the electrode, the aluminum layer is wet-etched and polysilicon layer is dry-etched, using a reactive ion etching (RIE) process with a mixture of tetrafluoromethane (CF_4) and O_2 plasma, according to the Mask layout. The structured polysilicon layer is oxidized at a temperature of 900°C in dry O_2 atmosphere to form the oxide layer which is sequentially etched by BOE solution [35]. The oxidation time is varied from 5 to 15 min in each cycle of oxidation and etching depending on the thickness of the polysilicon layer. The prepared structures are optically characterized with a SEM (JOEL) before and after the oxidation process.

2.3. Electrical Characterization. The final device with 90, 75 and 42 nm gap is connected to a dielectric analyzer (Alpha-A High Performance Frequency Analyzer, Novocontrol Technologies, Hundsangen, Germany). Capacitance, permittivity, and conductivity are measured at room temperature with air in the nanogap spaces.

3. Results and Discussion

3.1. Nanogap Fabrication. Figure 4 shows the photo Mask and the SEM cross-sectional view of an original photolithographically patterned polysilicon layer before and after applying the oxidation process. The thickness of the polysilicon layer plays an important role in the stability of the fabricated structure. According to our experience, fabricated structure is frequently broken down if a thin layer of polysilicon (<200 nm) is used. For the current experiment, a polysilicon layer of 2000 nm is chosen because of its higher stability in sequential thermal oxidation and etching. After patterning the polysilicon layer with the designed chrome Mask, the width of the layer at gap location is 1.228 μm (shown by cursor height in Figure 4(b)). Then we apply sequential thermal oxidation and etching in alternation to create a nanogap at the desired position. An oxide layer of silicon dioxide (SiO_2) is created on polysilicon layer (Figure 4(c)) by thermal oxidation at 900°C for 15 min [35], and then the fabricated oxide layer is stripped out completely (Figure 4(d)) by the etching process using buffer oxide etching (BOE) solution for 10–15 min [36].

Figures 5(a)–5(i), shows the nanogap structure at the end of each cycle of oxidation and etching. We observe that the polysilicon layer loses its width by 60–280 nm after each cycle of oxidation and etching, depending on the stages of cycles. Thus at the end of the 7th cycle, a 90 nm gap is realized (Figure 5(g)). We then reduce the oxidation time of the structure shown in Figure 5(f) from 15 min to 10 min. After etching with BOE solution for 10–15 min, we found a 75 nm gap (Figure 5(h)). We further reduce the time of oxidation to 5 min to obtain a 42 nm gap (Figure 5(i)). Repetition of the procedures in triplicate experiment generates a nanogap of diameter 42 ± 5 nm showing the feasibility of the method to be used in batch production.

The precise control of nanostructure dimensions is a crucial point for a reproducible fabrication [37]. The pattern size reduction technique can generate an excellent reproducibility by controlling the thickness of oxide layer [35]. Thus, the size of the nanogap structure can be precisely controlled by the careful selection of oxidation time. In order to see the relationship of the pattern-size reduction of the polysilicon layer with oxidation time of the 7th cycle, the thickness of the oxide layer and also the size of the fabricated gap are measured. A plot of layer thickness and oxidation time (Figure 6(a)), demonstrates a proportional relationship. Similar relationship is also observed between nanogap size and oxidation time when they are plotted in a graph (Figure 6(b)). A plot of nanogap size versus oxide layer thickness reveals that gap size is increased over the time of oxidation (Figure 6(c)).

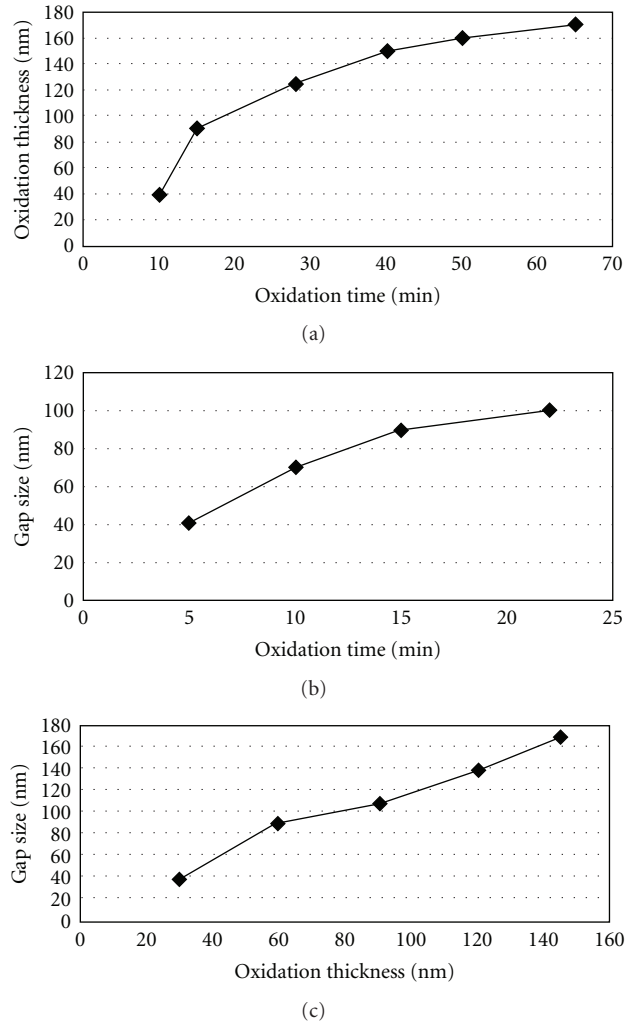

Figure 6: The thickness of oxide layer (a) and gap size (b) as a function of the 7th-cycle oxidation time. The relationship of gap size and oxidation thickness is shown in (c).

3.2. Electrical Properties of Fabricated Nanogap Electrodes. Electrical sensing of biomolecules (proteins and nucleic acids) solely relies on the measurement of current and/or voltage to identify target binding [38]. Usually a probe biomolecule is immobilized in the nanogap between the electrode pair, and electrical properties are measured to come up with a decision whether the detection is achieved or not [39]. Detection with low voltage or current is desired as high voltage may burn the anchored biomolecule probes and targets simultaneously, causing the device failure in biological sensing [40]. Gap-size reduction should allow the electrode structure to detect target biomolecule binding with very low supply of current.

Figures 7(a)–7(c), show the capacitance, permittivity, and conductivity parameters of 90, 75 and 42 nm gap electrodes fabricated in the current experiment. An increment of all three parameters, namely, capacitance, (a), permittivity, (b), and conductivity, (c), is achieved with the reduction of gap size. This can be explained with following

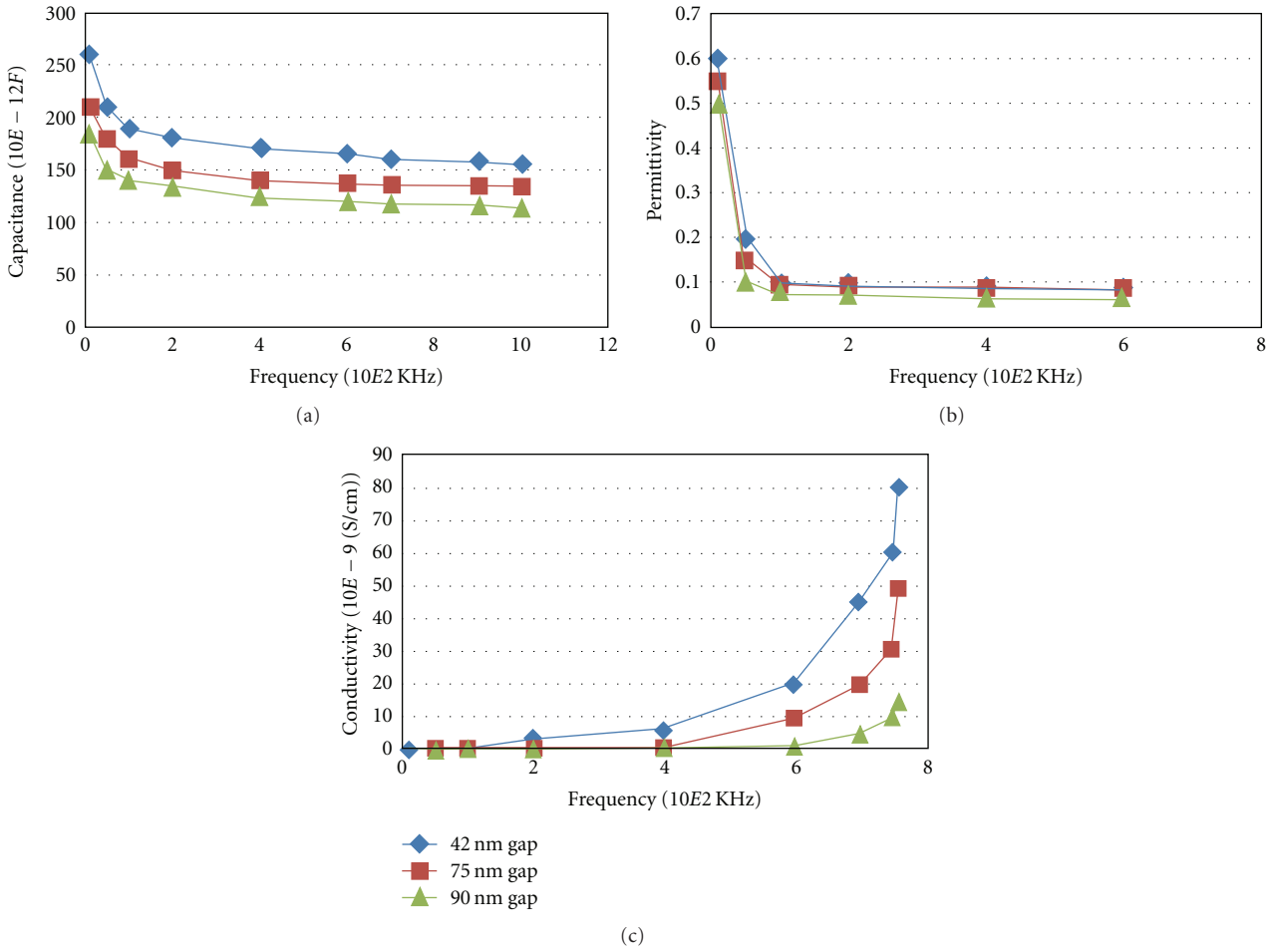

Figure 7: Capacitance (a), permittivity (b), and conductivity (c) profiles of different nanogap electrodes.

simple equation that explains the operating principle of a capacitor:

$$C = \frac{\acute{\varepsilon} * A}{d}, \tag{1}$$

where: $\acute{\varepsilon} = \varepsilon/\varepsilon^{\circ}$; $\acute{\varepsilon}$: the permittivity; ε°: the permittivity for air in the free space; C: the capacitance value; A: the surface area of the nanogap structure, and d: the size of the gap/distance between the two plates.

Since the gap size, d, is the denominator of the above equation, reduction of gap-size should increased the capacitance of a nanogap capacitor [41]. The equation also reflects that permittivity and capacitance have a linear relationship. Therefore, permittivity enhancement by gap-size reduction is a logical outcome.

Permittivity reflects the index of a material's ability to transmit current without imposing a resistance [42]. On the other hand, conductivity is a measure of a substance capacity to allow the passage of current. Thus, the relation of permittivity, and conductivity is proportional. Therefore, an increment of capacitance, permittivity and conductivity with gap-size reduction suggests that the fabricated nanogap structure can be used in biosensing applications with the minimum supply of power.

Nanogap structures are also implicated to eliminate the formation of electrical double layer between the electrodes in dielectric sensing of proteins and nucleic acids [33]. Dielectric detection of biomolecules is interesting as it is label-free and does not need any reference electrode [43]. In the current experiment, no dielectric measurement is performed as it can be done only after immobilizing the probe biomolecule in the appropriate nanogap. However, our group is working to do it in near future and will be reported in a separate publication.

3.3. Limitation and Efficacy of the Current Method. The current method of fabricating nanogap etches up the surfaces of the plates that separated the gap. More benefit of the desired properties can be realized if integrity of the polysilicon layer can be restored. However, the measurement of capacitance, permittivity, and conductivity clearly reflects certain advantages of the 42 nm gap structure over those of 75 and 90 nms showing its feasible operation with low-current supply. Moreover, the potential of the current method in reproducible fabrication of the desired nanogap has made it a suitable candidate in batch production.

4. Conclusion

A simple method for the fabrication of nanogaps of less than 50 nm in diameter using polysilicon material on a Si–SiO_2–Si_3N_4 substrate is developed. The method combines the conventional lithography and pattern-size reduction techniques to fabricate desired nanogap in a reproducible manner which is essential in batch production. Measurement of several electrical parameters strongly suggests that structure can be used in electrical devices that consume very low level of electricity. The fabricated structure should been abled to detect biomolecules with the minimal supply of electrical current.

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